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Lateral ZnO nanowire growth on a planar substrate using a growth barrier

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Abstract

In this work, we present a technique to confine zinc oxide (ZnO) nanowires to lateral growth while suppressing nanowire growth on the top surface of a planar substrate through the use of a growth barrier.
Physical-vapour-deposited silicon dioxide and spin-on-glass dielectric were evaluated, and both have proven themselves as effective growth barriers. Through a simple oxidation process, ZnO nanowires, with typical diameters in the range of 20–40 nm, will grow laterally from selectively exposed zinc edges on otherwise encapsulated zinc lines. X-ray diffraction measurements show that the as-grown nanowires belong to the crystalline hexagonal-structured ZnO. This simple and cost-effective fabrication process, coupled with its process compatibility with existing silicon technology and its scalable nature, is a viable processing technique to selectively grow lateral ZnO nanowires on a planar substrate, with potential applications in nanowire devices.

1. Introduction

In recent years, one-dimensional (1D) semiconductor nanostructures have received steadily growing interest due to their unique properties and potential for superior performance in various applications compared to their bulk counterparts [1, 2]. In particular, ZnO nanostructures, such as nanowires and nanorods, have become the focus of intensive research arising from several attractive properties of ZnO, such as a direct and wide band-gap, high crystalline quality, large exciton binding energy, and piezoelectricity [3, 4]. Nanodevices based on this material thus hold great promise for electronics, optoelectronics, and sensor applications [3–8]. While a significant amount of research effort concerns the rational synthesis of vertically aligned ZnO nanowires/nanorods, with good progress reported to date [5, 9–12], the synthesis of laterally aligned ZnO nanowires has received less attention. Recently, Kim *et al* [14] and Fan *et al* [13] reported the growth of lateral ZnO nanowires with different growth conditions. However, the ability to selectively grow these laterally orientated ZnO nanowires at predefined locations is not demonstrated in these reports. Nikoobakht *et al* [15] reported the predictable positioning of horizontal ZnO nanowires on a sapphire substrate by an elegant method, utilizing nanoimprint lithography to pattern gold catalyst lines on the substrate for subsequent ZnO nanowire growth by a vapour phase transport process. Conley *et al* [18] and Lee *et al* [16] demonstrated directly grown horizontal ZnO nanowires that bridge prefabricated electrodes, and which can be made into functional devices such as gas sensors or UV sensors.

Nevertheless, the ability to selectively grow lateral 1D nanostructures will be an important development since these laterally orientated nanostructures constitute the very basic building blocks for the realization of integrated nanoscale devices on a planar substrate [17]. Currently, the most common approach in fabricating planar ZnO nanowire devices employs the 'pick and place' method, whereby ZnO nanowires grown *ex situ* on a separate substrate are 'harvested' and redeposited onto the device substrate before being individually contacted by electrodes delineated by electron-beam lithography, or focused-ion-beam deposition to form external electrical interconnects [3, 7, 19–21]. Due to the random nature of the redeposition process, it is difficult to dictate the exact placement of the laterally dispersed nanostructure on the device substrate. Although some degree of control over the lateral alignment of the nanowire could be achieved through the use of electric-field-assisted assembly or fluidic flow alignment [22–24], the extra processing steps complicate the

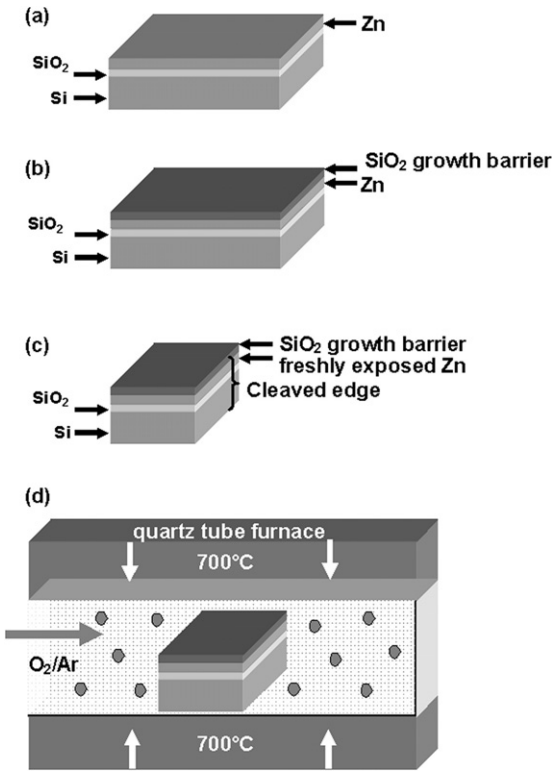

Figure 1. Schematic diagram of process flow used in PVD SiO_2 growth barrier evaluation with an unpatterned die. (a) Thermal evaporation of Zn. (b) RF sputter deposition of SiO_2 growth barrier. (c) Cleaved die. (d) Thermal oxidation of cleaved die.

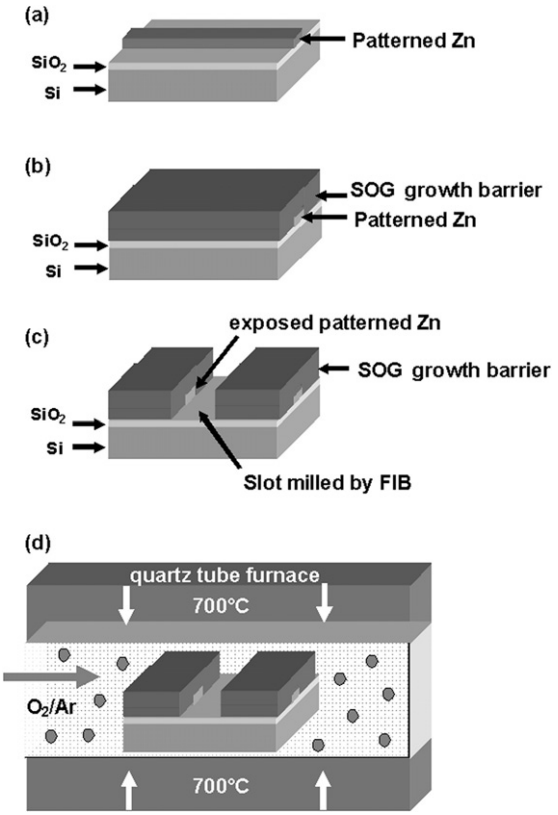

Figure 2. Schematic diagram of process flow used in SOG growth barrier evaluation on a patterned chip. (a) Zn electrode delineated by electron-beam lithography, after metallization and lift-off. (b) SOG growth barrier deposition by spin coating. (c) Ion milling by FIB to etch a slot to expose part of the patterned Zn. (d) Thermal oxidation.

overall device fabrication. The general drawbacks of the 'pick and place' method, such as the tedious and time-consuming processing steps, as well as its non-scalable nature, make it an impractical method to fabricate planar nanowire devices, let alone for large-scale manufacturing to realize integrated nanoscale devices.

We recently reported a technique to grow ZnO nanowires at predefined locations on an insulated silicon substrate using an *in situ* growth process [25]. Using this technique, a planar nanowire-based photodetector was fabricated, demonstrating a simpler alternative to the conventional 'pick and place' method for the fabrication of nanowire-based devices. In this work, we report an improvement of this growth technique—by the use of a growth barrier—to confine the growth of ZnO nanowires laterally on a planar substrate. Two types of growth barrier are evaluated, namely physical-vapour-deposited silicon dioxide (PVD SiO_2) and spin-on-glass (SOG) dielectric. In addition, a patterned chip was used to show selective growth of the nanowires due to its self-catalytic growth nature. X-ray diffraction (XRD) analysis revealed that the nanowires grown are ZnO, and belong to the crystalline hexagonal-structured ZnO.

2. Sample preparation

To evaluate the effectiveness of PVD SiO_2 as a growth barrier layer, an unpatterned die was used to illustrate the proof of concept. A 5 mm × 5 mm SiO_2 insulated silicon die was blanket deposited with Zn metal (figure 1(a)). The Zn metal was approximately 100 nm thick and deposited by thermal evaporation (BOC Edwards, Auto 306 Vacuum Evaporator) using 99.9999% Zn metal wire as the source material. As it is known that Zn does not normally form a deposit onto SiO_2 surfaces during evaporation unless aided by a pre-nucleant such as a small deposit of gold (Au) or silver (Ag) [26, 27], a thin layer of Au (∼4 nm) was deposited onto the die prior to Zn deposition. This was followed by a 200 nm thick SiO_2 barrier layer deposited using an RF sputtering system (Denton Discovery-18, RF Sputtering System) at an RF power of 100 W, with an argon gas flow of 100 sccm (figure 1(b)). Next, the die was cleaved (figure 1(c)). It is noted that one could not evaluate the effectiveness of the barrier layer fairly by using the edges of the uncleaved die due to the irregular coverage of the die edges by the zinc and SiO_2. The cleaved die was then placed in the middle of a quartz tube furnace and heated to 700 °C at atmospheric pressure, with an oxygen (O_2) and argon (Ar) gas flow in the ratio of 1:4, for a duration of two hours (figure 1(d)). After thermal oxidation, the die was observed using a field-emission scanning electron microscope (FE-SEM) (Phillips XL30 FEG).

A growth barrier based on SOG was also evaluated on a separate 5 mm × 5 mm SiO_2 insulated silicon die. In addition, the zinc film was patterned in order to demonstrate the selective growth of the nanowires. The die was patterned

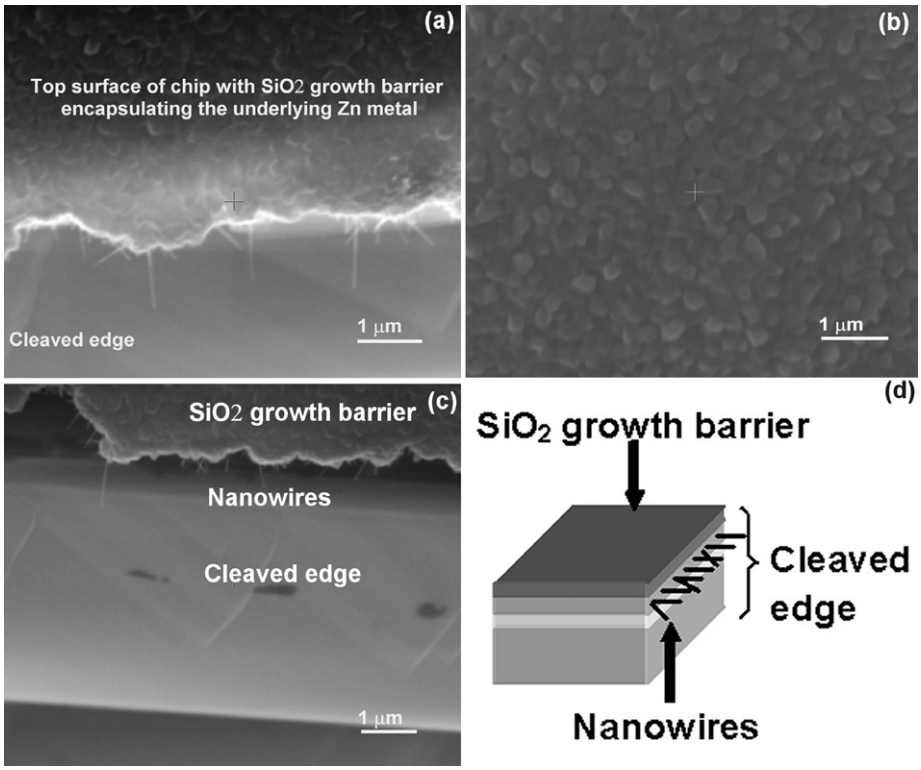

Figure 3. SEM micrographs of the unpatterned die used in the PVD SiO_2 growth barrier evaluation immediately following thermal oxidation. (a) (Top view) Nanowires grown laterally from the cleaved edge of the die. (b) (Top view) The top layer of the die did not show any signs of nanowire growth. (c) (15° tilted view) Cross-sectional view of the edge of the cleaved die shows selective growth of the nanowires only at the exposed Zn layer. (d) Schematic representation of the unpatterned die after thermal oxidation.

with lines of widths ranging from 4 to 10 μm, using polymethylmethacrylate (PMMA) resist and electron-beam lithography (note that coarse lithography with a photomask could also be utilized since the dimensions involved are relatively large). Pre-nucleant Au metal followed by Zn were then deposited using the same thermal evaporation conditions and equipment as those used for the evaluation of the PVD SiO_2 growth barrier described above, and lifted off in acetone, to define the zinc metal electrodes (figure 2(a)). Next, the chip was spin coated with liquid SOG (Honeywell, Acuglass® T12B) as the barrier layer (figure 2(b)). The thickness of the deposited SOG was approximately 180 nm. The SOG was cured at 120 °C in a convection oven for 3 h. Next, a focused ion beam (FIB) (FEI Quanta 200-3D) was used to mill a slot across the electrode in order to expose the patterned Zn metal on the side (figure 2(c)). The chip was then subjected to similar thermal oxidation conditions as those used in the evaluation of the SiO_2 growth barrier (figure 2(d)). Following thermal oxidation, the chip was observed in the FE-SEM.

The nanowires grown using each type of growth barrier were characterized using x-ray diffraction (XRD, Bruker GADDS) with Cu Kα radiation, to determine whether the nanowires grown are really ZnO and to examine their crystal structure.

3. Results and discussion

Figure 3 shows the SEM micrographs of the unpatterned die used in the PVD SiO_2 growth barrier evaluation immediately following thermal oxidation. The top-view SEM micrograph shows that nanowires grew laterally from the cleaved edge of the die where the Zn metal had been exposed by cleaving (figure 3(a)), whereas the top layer of the die with the Zn metal encapsulated by the SiO_2 layer did not show any signs of nanowire growth from the top surface (figure 3(b)). A cross-sectional view of the die (figure 3(c)) illustrates the selective growth of the nanowires only at the exposed Zn layer at the edge of the die. The diameters of the nanowires grown are around 20–40 nm. The inclination of these as-grown nanowires ranges from 0° (i.e. parallel to the substrate plane) to about 26° with respect to the substrate plane. Figure 3(d) is a schematic representation of this die. The results show the effectiveness of the PVD SiO_2 layer as a growth barrier to confine the growth of nanowires laterally on a planar substrate.

Figure 4 shows SEM micrographs of the patterned die used in the SOG dielectric growth barrier evaluation right after thermal oxidation. Nanowires were grown laterally only at the edges of the patterned region where the Zn metal had been exposed by ion milling (figure 4(a)), whereas the top layer of the chip being encapsulated by the SOG barrier layer did not show any evidence of nanowire growth (figure 4(b)). (The few ZnO nanowires grown on the top edge of the pattern were caused by FIB over-milling of the SOG layer, causing the Zn metal on the top to be slightly exposed during thermal oxidation.) The typical diameters and inclination of these as-grown nanowires are the same as the nanowires grown using the SiO_2 growth barrier. Figure 4(c) is a schematic representation of this die.

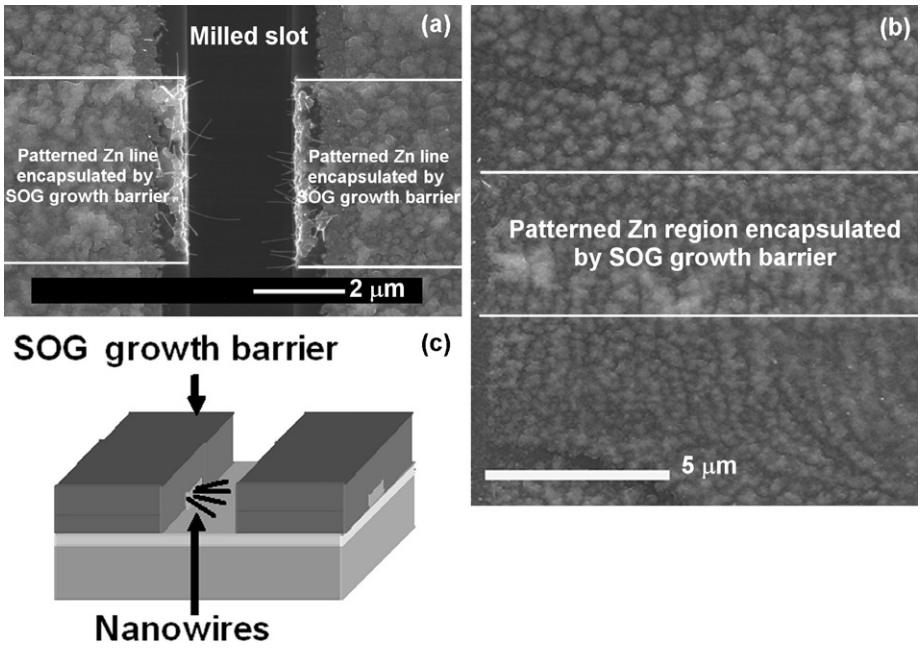

Figure 4. SEM micrographs of the patterned die used in the SOG dielectric growth barrier evaluation right after thermal oxidation. (a) (Top view) Nanowires grown laterally only at the edges of the patterned region where Zn had been exposed by ion milling. (b) (Top view) The top layer of the die shows no nanowire growth at the patterned Zn region. (c) Pictorial illustration of the patterned die after thermal oxidation.

Selective growth of the ZnO nanowires is possible in part due to the nature of nanowire growth by direct oxidation. The proposed growth mechanism has been reported in [25]. In brief, the growth is postulated to be self-catalytic, whereby the deposited patterned Zn simultaneously acts as both reactant and catalyst and reacts with the oxygen gas ambient when heated above its melting point to form ZnO nanoclusters. These ZnO nanoclusters, residing at the apices of the hexagonal shaped Zn grains, act as nucleation sites for the preferential growth of the nanowires along the edges of the hexagonal Zn grains. Moreover, the poor wettability of the ZnO with the Zn promotes the 1D growth of nanowires. TEM results also show that the nanowires grown are single crystalline with *a*-axis growth direction. However, using our previous method, which is without the use of a growth barrier, ZnO nanowires are grown on the top of the patterned Zn electrode as well as from the edges, as shown in figure 5. Recent reports by Conley *et al* [16] and Lee *et al* [17] demonstrating bridging of ZnO nanowires between two electrodes also face the same issue of growth on the electrode's top surface. Although this is not currently a concern for single-layer nanostructure integration, top-surface growth is not desirable for future integrated nanocircuits where several layers of vertical integration might be necessary. Thus, the use of a growth barrier could provide a possible solution to avoid this issue.

The nanowires grown using both types of growth barrier were analysed in an x-ray diffractometer. Figures 6(a) and (b) show the XRD patterns from the samples using the SiO_2 growth barrier and the SOG growth barrier, respectively. Within the measurement range, all the peaks in the JCPDS file for hexagonal-structured ZnO can be identified in both XRD patterns. This reveals that the product is composed of hexagonal-structured ZnO (space group: $P63mc$; a = 0.3242 nm, c = 0.5188 nm). Other peaks that are identified in the XRD patterns belong to hexagonal Zn and cubic Au. The existence of the Zn peak is due to the deposited Zn metal grains residing beneath the growth barrier that did not react with the gas flow. From another perspective, it also shows the effectiveness of these two materials as growth barriers—that is, to prevent growth at the undesired locations as intended. The presence of the Au peak is expected since these samples had been prepared with an underlying thin layer of gold to act as a pre-nucleant to allow Zn deposition onto the SiO_2 surface of the die.

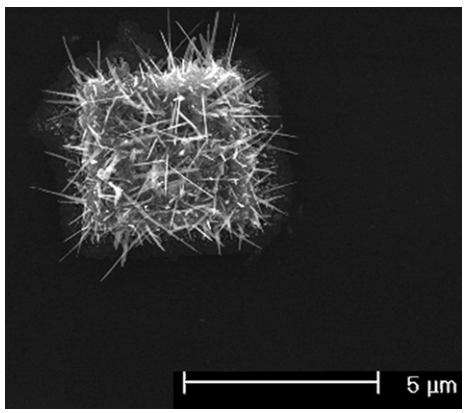

Figure 5. SEM micrograph showing ZnO nanowires grown on the top of the patterned electrode as well as from the edges without the use of a growth barrier.

For any new technology to be successfully rolled out to a manufacturing environment, process compatibility with existing well-established silicon technology is important. Therefore, the synthesis of 1D structures, being a relatively

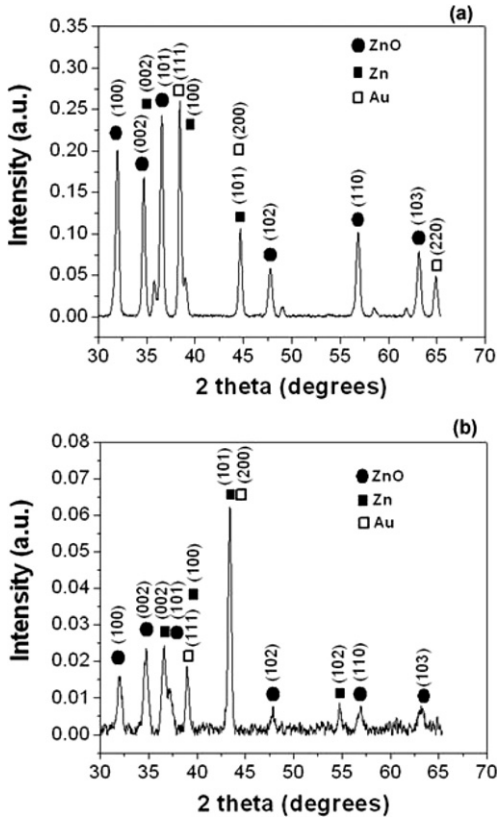

Figure 6. XRD patterns of the samples after thermal oxidation. (a) Sample with SiO_2 growth barrier. (b) Sample with SOG growth barrier. The difference in the intensity of the peaks of the two graphs is due to a weaker signal for the sample with SOG growth barrier where the amount of (patterned) zinc is lower.

new technology, will have to be integrated, at least initially, into the traditional top-down silicon-based platform. The two proposed growth barrier layers used in our work are typical materials used in the silicon industry, which allows fabrication-process compatibility using existing silicon technology-based equipment and recipes. In addition, the process using SOG as a growth barrier offers a more attractive fabrication technique since it is generally accepted that an SOG process is a much simpler and lower-cost process (in terms of equipment and material costs) compared to a PVD SiO_2 process [28]. Nonetheless, the technique proposed is scalable (although FIB is used to etch the patterned die for this proof of concept, in principle, plasma processing with suitable etch chemistry, e.g. CF_4 or SF_6 for SiO_2 or SOG etching [29] and CH_4/H_2 for Zn etching [30]) can be used, while the other processes needed are mainly standard processes such as lithography and evaporation). A potential application of these laterally orientated ZnO nanowires is as a directly assembled and integrated nanowire photodetector [25] where an array of such planar nanodevices could be fabricated across an entire wafer due to its scalable nature. The ability to grow ZnO nanowires laterally at the edge of a chip may also allow this technique to be used to fabricate an array of edge-emitting nanowire lasers/LEDs on a planar chip. In addition, the advantages of using such a technique will become more apparent in future integrated nanocircuits where the growth barrier can provide isolation among nanostructures built horizontally and/or vertically across the integrated chip.

4. Conclusion

A technique to confine ZnO nanowires to grow laterally on a planar substrate using a growth barrier such as PVD SiO_2 or SOG dielectric has been demonstrated. Using a patterned die, it has been shown that selective lateral growth of the nanowires is also possible. XRD measurements show that the nanowires grown are crystalline hexagonal-structured ZnO. The two proposed growth barriers are typical materials used in existing well-established silicon fabrication technology which allows them to be process compatible using extant silicon-based equipment and recipes, though the SOG growth barrier appears to be a more attractive candidate as it involves a simpler and cheaper process. In addition, the technique proposed is scalable, making it a viable processing approach to selectively grow lateral ZnO nanowires on a planar substrate, which may find application in devices such as nanowire photodetectors and edge-emitting lasers, as well as for future integrated nanocircuits.

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